

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

Claim 1 (**Currently amended**): A method of testing a memory device for determining operating life with stressing, comprising:

cycling through each address of the memory device by generating a respective bit pattern comprised of a predetermined number of bits including row and column address bits for each address;

applying stressing signals on a respective at least one cell of the memory device corresponding to each generated address in the cycling;

wherein each of all possible row and column addresses of the row and column address bits is cycled through for application of the stressing signals;

performing the cycling and the applying of the stressing signals for a predetermined stress time period; and

minimizing charge gain failure in the memory device after the predetermined stress time period with a transition of less than the predetermined number of bits for sequencing to each subsequent address during the cycling.

Claim 2 (**Previously Presented**): The method of claim 1, further comprising:
cycling through the respective bit pattern for each of the addresses in a gray code sequence.

Claim 3 (**Previously Presented**): The method of claim 2, wherein the memory device is a flash memory device.

Claim 4 (**Previously Presented**): The method of claim 3, wherein the stressing signals include a clock signal applied on a respective word line corresponding to each generated address,

and include a bit line voltage applied on a respective at least one bit line corresponding to each generated address.

Claim 5 (Previously Presented): The method of claim 2, further comprising:
generating a respective binary bit pattern for each of the addresses;
converting the respective binary bit pattern to a respective gray code bit pattern for each of the addresses; and
using the respective gray code bit pattern for the cycling.

Claim 6 (Previously Presented): The method of claim 2, further comprising:
heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device.

Claim 7 (Previously Presented): The method of claim 1, further comprising:
cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address.

Claim 8 (Previously Presented): The method of claim 1, wherein the memory device is a flash memory device.

Claim 9 (Previously Presented): The method of claim 8, wherein the stressing signals include a clock signal applied on a respective word line corresponding to each generated address, and include a bit line voltage applied on a respective at least one bit line corresponding to each generated address.

Claim 10 (Previously Presented): The method of claim 1, further comprising:
heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device.

Claim 11 (**Currently Amended**): A system for testing a memory device for determining operating life with stressing, comprising:

an address generator for cycling through each address by generating a respective bit pattern comprised of a predetermined number of bits including row and column address bits for each address;

signal generators for generating stressing signals applied on a respective at least one cell of the memory device corresponding to each generated address in the cycling;

wherein each of all possible row and column addresses of the row and column address bits is cycled through for application of the stressing signals;

and wherein the cycling and the applying of the stressing signals are performed for a predetermined stress time period; and

means for minimizing charge gain failure in the memory device after the predetermined stress time period with a transition of less than the predetermined number of bits for sequencing to each subsequent address during the cycling.

Claim 12 (**Previously Presented**): The system of claim 11, further comprising:

a gray code converter for cycling through the respective bit pattern for each of the addresses in a gray code sequence.

Claim 13 (**Previously Presented**): The system of claim 12, wherein the memory device is a flash memory device.

Claim 14 (**Previously Presented**): The system of claim 13, wherein the signal generators include:

a clock signal generator for generating a clock signal applied on a respective word line corresponding to each generated address; and

a bit line voltage generator for generating a bit line voltage applied on a respective at least one bit line corresponding to each generated address.

Claim 15 (**Previously Presented**): The system of claim 12, wherein the address generator generates a respective binary bit pattern for each of the addresses, and wherein the gray code converter converts the respective binary bit pattern to a respective gray code bit pattern for each of the addresses, and wherein the system further comprises:

address decoders for decoding the respective gray code bit pattern for determining the respective at least one memory cell to have the stressing signals applied thereon.

Claim 16 (**Previously Presented**): The system of claim 12, further comprising:
a heater for heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device.

Claim 17 (**Previously Presented**): The system of claim 11, further comprising:
means for cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address.

Claim 18 (**Previously Presented**): The system of claim 11, wherein the memory device is a flash memory device.

Claim 19 (**Previously Presented**): The system of claim 18, wherein the signal generators include:

a clock signal generator for generating a clock signal applied on a respective word line corresponding to each generated address; and

a bit line voltage generator for generating a bit line voltage applied on a respective at least one bit line corresponding to each generated address.

Claim 20 (**Previously Presented**): The system of claim 11, further comprising:
a heater for heating the memory device during the predetermined stress time period for HTOL (high temperature operating life) testing of the memory device.